PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of	Docket No: Q57908
Takao TOI	
Appln. No.: 09/505,429	Group Art Unit: 2623
Confirmation No.: 7134	Examiner: Colin M. LAROSE
Filed: February 16, 2000	
For: IMAGE PROCESSING SYSTEM	

REPLY BRIEF PURSUANT TO 37 C.F.R. §41.41

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. § 41.41, Appellant respectfully submits

this Reply Brief in response to the Examiner's Answer dated March 18, 2005. Entry of this

Reply Brief is respectfully requested.

ARGUMENT

A.   Grouping of Claims

The Examiner asserts that the rejection of claims 1-22 stand or fall together because

appellant's brief does not include a statement that this grouping of claims does not stand or fall

together and reasons in support thereof. The Examiner refers to 37 C.F.R. § 1.192(c)(7) for

support. However, the appellate rules changed as of September 13, 2004 and a statement

regarding grouping is no longer required. See 37 C.F.R. § 41.37. Appellant has fully complied

with 37 C.F.R. § 41.37 and has provided separate arguments for claims 1-20 (as a group), 21 and

22.

B.   Response Regarding Claims 1-20

1.   Kolchinsky Does Not Disclose the Claimed Digital Control Processing

The Examiner asserts zooming and panning are well-known terms of art that refer to

operations for controlling the position of a camera lens and camera head. However, the

Examiner provides no support for that assertion. Appellants do not disagree that panning and

zooming can refer to controlling the position of a camera and camera head. However, that is not

the only meaning of those terms. For example, zooming can refer to the process of enlarging the

size of an image on a computer (e.g., the zoom feature in Adobe Acrobat Reader or Mapquest).

Neither of those two examples involves controlling a camera. Likewise, the zooming and

panning in Kolchinsky involves the manipulation of an image and not the control of a camera.

The Examiner also "presumes" that the "image acquisition" function in Kolchinsky

figure 4 refers to an operation for controlling the acquisition of an image, such as turning a

camera on and off. This is pure speculation. A more reasonable reading of Kolchinsky is that

the image is acquired from the image data bank 24 (see figure 2) that is in the reconfigurable

sequential processor 12. There is no disclosure or suggestion in Kolchinsky of controlling any

external hardware such as a camera.

2.   Kolchinsky Does Not Suggest Combining a Digital Image Processor with a Digital Control Processor

As mentioned in Appellant's opening brief, the Examiner concedes that Baxter et al. fails

to disclose an FPGA for executing the image and control processing wherein the first and second

internal logic descriptions, corresponding to each type of processing, are written to the FPGA.

See also Examiner's Answer at page 4. To make up for this deficiency, the Examiner cites to

Kolchinsky and argues that "Kolchinsky is describing the exact situation found in Baxter

wherein separate processors perform separate operations relating to video data, and each

processor is only being utilized part of the time - either during the active interval or the non-

active interval." The Examiner cites to col. 1, lines 17-29 for support.
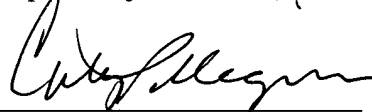
Appellant disagrees that Kolchinsky describes the situation in Baxter because Kolchinsky

fails to disclose digital control processing for the reasons described above. Kolchinsky discloses

merging multiple digital image processors, but it does not disclose merging digital control

processors with digital image processors. As mentioned in Appellant's opening brief, the digital

camera processor 66 must execute processes faster, and CPU 70, which is a general purpose

processor, is not suitable for controlling the camera. Therefore, in order to combine processor 66

and CPU 70, it would be necessary to use a wired logic processing device, such as an ASIC,

instead of a general purpose CPU. Because the processing requirements for image processing

and control processing are different, Kolchinsky would not suggest to one skilled in the art to

combine processors 66 and 70 into one FPGA.

CONCLUSION

For the above reasons as well as the reasons set forth in Appeal Brief, Appellant

respectfully requests that the Board reverse the Examiner's rejections of all claims on Appeal.

An early and favorable decision on the merits of this Appeal is respectfully requested.

Respectfully submitted,

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